

10/813,240

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT M. HORIGUCHI, et al.	
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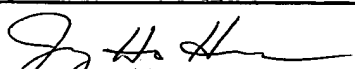
U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
JA	AA 4,675,845	6/87	Itoh, et al.	365	51	
JA	AB 4,389,715	6/83	Eaton, Jr., et al.	365	200	
JA	AC 4,727,516	2/88	Yoshida, et al.	365	200	
JA	AD 4,648,075	3/87	Segawa, et al.	365	200	
JA	AE 4,837,747	6/89	Dosaka, et al.	365	200X	11/30/97
JA	AF 5,265,055	11/93	Horiguchi, et al.	365	200	10/10/89
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JA	AJ 4,752,914	06/88	Nakano et al	365	200	
JA	AK 6,577,544	06-03	Horiguchi et al	365	200	
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FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
JA	AM 60-130139	11/85	Japan				X
JA	AN 62-40700	2/87	Japan			X	
JA	AO 59-135700	8/84	Japan			**	
	AP		**see listing AH above				
	AQ						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

JA	AR	IEEE Journal of Solid-State Circuits, Vol. SC-16, No. 5, October 1981, pp. 479-487.
JA	AS	IEEE PROC., Vol. 130, Pt. I, No. 3, June 1983, pp. 127-135.
JA	AT	1984 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 282-283.
JA	AU	IEEE Journal of Solid-State Circuits, Vol. 26, No. 1, January 1991, pp. 12-17.
JA	AV	"System for Efficiently Using Spare Memory Components for Defect Corrections Employing Content-Addressable Memory." IBM Technical Disclosure Bulletin, vol. 28, no. 6, November 1985, pp. 2562-2567.
Examiner 		Date Considered 7/23/04